# Design of High-Speed Fiber Optic Datalinks

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*Abstract* — **Fiber-optic datalinks operating at rates of OC-48 (2.5Gb/s), OC-192 (10Gb/s), OC-768 (40Gb/s), and 10Gigabit Ethernet (10.3 Gb/s) utilize high-speed broadband electronic components, and require a combination of microwave, high-speed digital, and fiber-optic design techniques. In this paper, an overview of such high-speed fiber optic devices is given, concentrating on "Metro" (metropolitan area network) 10Gb/s applications, as this is currently an active area of industry activity. Tradeoffs between different high-speed process technologies will be discussed, as well as trends in the industry.**

## I. Introduction

High-speed electronic chipsets are ubiquitous in today's telecommunications equipment. Figure 1 shows how these high-speed chipsets are sometimes designed directly onto line cards, which then go into a system rack. However, in recent years a subsystem market has developed, in which increasing functionality is put into a subsystem product, which is then integrated into a line card through a standardized interface.

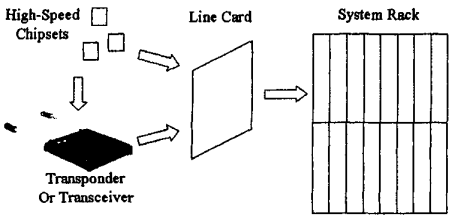


Fig. 1. System block diagram. High-speed chipsets are sold directly into the line card market, as well as the integrated transponder / transceiver market.

In this way the telecommunications market has become a horizontal market in some segments, particularly for short-distance communications links, where mass-produced standardized fiber-optic subsystems offer a low-cost, reliable alternative to high-speed component integration directly on the line card. Such a standardized subsystems approach offers a significant time-to-market advantage to systems companies, while saving engineering development resources.

## II. The 300-Pin 10Gb/s Transponder

A transceiver generally consists of a fiber-optic transmit and receive pair. For the highest-speed datarates, it is popular to include Serializer / Deserializer (SerDes, or so-called Mux / Demux) functionality into these devices, which are then called a "transponder", or "SerDes transceiver". An example of such a device is the 300-pin MSA (multi-source agreement) transponder, shown in Figure 2. Such a device takes a serial datastream into and out of a singlemode fiber pair and converts the fiber signal into several parallel electronic data channels. This allows electronic equipment to interface to the device at lower individual channel bitrates. The transponder contains several high-speed electronic chips which process the digital signal before it is launched onto a fiber link, as well as monitor and control signals which control key functions and give the system important data about the operation of the datalink. This 300-pin transponder product supports both short-reach (up to 12km) and intermediate-reach (up to 40km) applications, with next-generation versions of this device extending to 80km and DWDM applications.

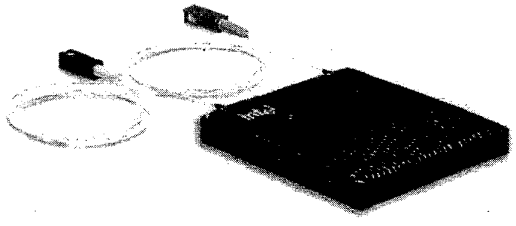

Fig. 2. Intel fiber-optic transponder product with 10Gb/s fiber inputs / outputs, and parallel 16-bit 622Mb/s electrical interface (through 300-pin connector, bottom of device). This device meets SONET, 10GbE, and FEC rate / protocol requirements.



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In the case of the 300-pin MSA 10Gb/s transponder, a multiplexer chip takes a parallel 16-bit 622Mb/s electrical signal and converts it to a serial 10Gb/s electrical data signal. A demultiplexer chip conversely takes a serial 10Gb/s electrical signal, recovers the clock, and generates a parallel 16-bit 622Mb/s data stream output (together with a clock). The 10Gb/s multiplexer and demultiplexer chipset is usually fabricated using GaAs, Bipolar Silicon, SiGe, or (more recently) CMOS processes, with SiGe and CMOS processes having the potential to move to higher levels of integration. Figure 3 shows a block diagram for an example 300-pin transponder design (the Intel TXN13300). This particular transponder has a bipolar silicon serializer / deserializer chipset (Intel LXT16784 / LXT16785), while the packaged driver amplifier is fabricated utilizing GaAs, and the TIA (transimpedance amplifier) inside the receiver optic utilizes SiGe. Clearly several different process technologies coexist in today's designs. In this example silicon, silicon germanium, and gallium arsenide high-speed IC's, as well as the InP (Indium Phosphide) transmit and receive lasers, coexist within one transponder product.

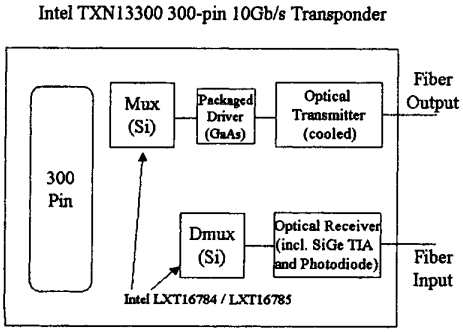


Fig. 3. Block diagram for Intel TXN13300 10Gb/s 300-pin transponder.

The 10Gb/s output from the multiplexer must be amplified to generate enough voltage / current to drive the modulated laser device, and therefore a high-speed driver is a key component of the transponder product. Such a driver generally takes a 0.5Vpp (50ohm) signal and amplifies it to 3Vpp (50ohms), or higher. Such drive amplifiers must have frequency response from around 10kHz to beyond 10GHz in order to preserve the integrity of the high-speed digital data stream. Generally, GaAs or SiGe processes are used for high-speed drivers, although CMOS can be used for some driver applications. Figure 4 shows a 10Gb/s transmit eye generated by the Intel TXN13300 300-pin MSA transponder; the eye starts at the Silicon multiplexer, becomes amplified by the GaAs drive amplifier, and then goes through the InP laser diode to the fiber (in this case it is a directly modulated, cooled DFB (Distributed Feedback) laser).

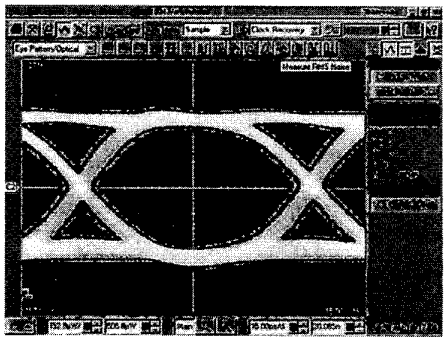

Fig. 4. Transmit eye of Intel 300-pin MSA transponder at 10Gb/s.

On the receiver side, a low-noise transimpedance amplifier (TIA) takes the current from a high-speed photodiode and generates an amplified voltage signal, which is then fed into a limiting amplifier (or automatic gain-control amplifier) to generate enough signal amplitude to drive the demultiplexer / CDR (clock and data recovery circuit) input. In the case of the TIA, stable gain with flat frequency response is again necessary, although low-noise performance is paramount instead of high-voltage swing capability. Several processes are used for TIA's, including SiGe, GaAs, and CMOS.

In addition to the high-speed electronic components themselves, transmission lines and high-speed interfaces are used to connect the high-speed components to each other, which must all be designed with careful attention to loss, reflection, crosstalk, and other electromagnetic effects. In most cases, the DC signal level of the various components are incompatible, which requires the interface between them to have a DC blocking capacitor -- which again must have flat frequency response from around 10kHz to beyond 10GHz (in the case of OC-192 or 10Gigabit Ethernet), and beyond 40GHz in the case of OC-768. Many of the techniques used are surprising to the standard microwave designer (such as the use of standard FR-4 "green" PC Board material to transmit 10Gb/s signals over short distances).

Design challenges include high-speed interface design, EMI compliance, meeting eye diagram compliance, receiver sensitivity, jitter generation, jitter tolerance, jitter transfer, and ensuring that all monitor and control functions work accurately and reliably over temperature and all other operating conditions.

## III. SMALL-FOOTPRINT 10GB/S TRANSPONDERS

Telecommunication system vendors are increasing their port density (total data throughput per volume), at the same time that cost is becoming paramount due to market pressures. To address this need, transponder subsystem vendors are introducing small-footprint transponders. For example, the Intel 300-pin transponder introduced in section II is 3.5"x4"x0.53" in size, whereas Intel and other vendors are now introducing 300-pin transponders which are 2.2"x3"x0.53" in size (Intel TXN13200), utilizing approximately half of the line card space in a customer system.

A new small form factor MSA (multi-source agreement) transponder is being introduced specifically for 10GbE applications (the XENPAK transponder, see Figure 5). The XENPAK device is not only very narrow (approximately 1.4" wide), but it also allows hot-pluggability (systems can be upgraded "on the fly"), as well as direct front-face line card mounting. The electrical interface is called "XAUI" (pronounced "zowee"), and consists of four 3.125Gb/s electrical signals (as opposed to the 16 electrical signals used in the 300-pin transponder), which allows the device's narrow width.

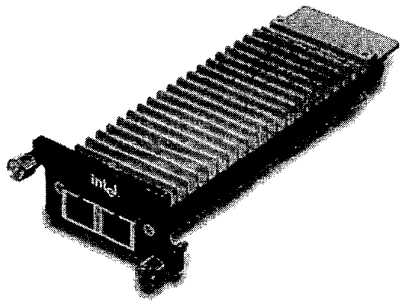

Fig. 5. XENPAK 10GbE small form-factor transponder product.

The new smaller transponder footprints require several internal changes to the design. Paramount among these changes is reduced power consumption. Mid-sized 300-pin transponders have maximum power dissipation in the range of 8-9W (in the case of the Intel TXN13300), or sometimes as high as 12W or higher for some vendor offerings (especially for longer-reach applications). Both the small footprint 300-pin transponder (Intel TXN13200) and the small footprint XENPAK transponder (Intel TXN17401) have maximum power dissipation around 6W, which depends on two key factors: low-power high-speed chipsets, and utilizing an uncooled transmit laser. The uncooled transmit laser saves between 1W-3W relative to TEC-cooled lasers, depending on the specifics of the TEC circuits used in cooled designs. Also of high importance is the use of custom small form factor optic modules, and the increasing use of more highly integrated high-speed IC's (removing as many components as possible from the PC board saves precious PCB area, reduces component cost, and increases reliability).

The block diagram for small-footprint transponders is shown in Figure 6. A low-power multiplexer / demultiplexer chipset is utilized (this part of the chipset depends upon the 16-bit 300-pin vs. 4-bit XAUI application). An uncooled laser diode is used, which allows the TEC circuit to be eliminated (saving power as mentioned above). For these small form factor transponders, the drive amplifier is integrated into the transmit optic in die form, which allows the use of a non-50ohm impedance and a short electrical interface between the driver output and the transmit laser. This low-impedance interface saves power dissipation and allows higher current swing for a given voltage swing. The drive amplifier integration into the transmit optic saves PCB space and saves on die packaging cost. The receiver is also packaged into a small form factor optic module.

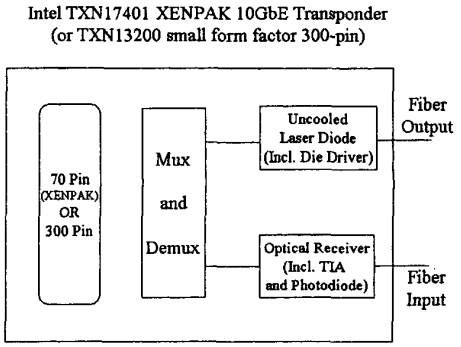


Fig. 6. Small form-factor 10Gb/s transponder block diagram (XENPAK or 300-pin).

As cost is becoming increasingly critical, particularly for 10GbE applications, directly modulated 10Gb/s multimode VCSEL laser diodes are gaining popularity for VSR (very-short-reach) applications below 300 meters in small footprint transponders. XENPAK will accommodate such multimode VCSELs, for instance. Since VCSELs require very low drive currents, this is an application for which a CMOS-based drive amplifier can be used.

## IV. NEXT-GENERATION: 40GB/S

Next-generation transponders will operate at 40Gb/s (OC-768) and higher serial datarates, and will require a new breed of even higher bandwidth IC's to enable them. For adoption of 40Gb/s over 10Gb/s, the power dissipation (and therefore size), as well as price, for a 40Gb/s transponder must become significantly less than four times the power and price of a 10Gb/s transponder – and the high-speed electronics behind the transponder (framers and other devices) must operate four times as fast as well.

Figure 7 shows an example block diagram for a short-reach serial 40Gb/s 300-pin transponder using an EA (electro-absorption) modulator. The multiplexer and demultiplexer chipset in this case takes a parallel 2.5Gb/s signal and converts it to a serial 40Gb/s signal. Figure 8 shows a measured 40Gb/s eye diagram from a high-speed electro-absorption modulator.

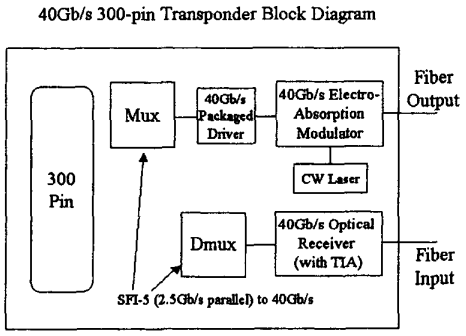


Fig. 7. Example 40Gb/s 300-pin transponder block diagram.

Interconnect issues become much more severe as data rates increase from 10Gb/s to 40Gb/s and beyond. For example, in Alumina (a material commonly used in high-speed optic components), a resonant half-wavelength at 40GHz is on the order of only one millimeter. Therefore, electrical packaging design will become more critical for 40Gb/s systems, requiring more extensive 3-dimensional electromagnetic simulation, and careful interconnect strategies.

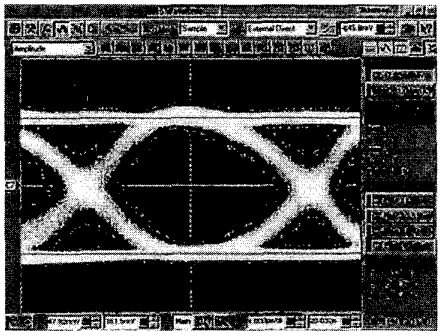

Fig. 8. 40Gb/s eye diagram from a high-speed electro-absorption (EA) modulator.

## V. CONCLUSION

High-speed IC's are used extensively in fiber-optic networks: directly on line cards, as well as in integrated fiber-optic subsystem (transponder or transceiver) products. Several process technologies coexist in these systems, with strengths of each being exploited for particular applications. High-speed microwave knowledge and design techniques are required for the successful integration of these high-speed IC's into fiber-optic systems.

## ACKNOWLEDGEMENT

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